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#ISC20

Italian National Agency for New Technologies, Energy and Sustainable Economic Development

Using High-Level Synthesis to Implement the Matrix-Vector Multiplication on FPGA

Alessandro Marongiu, Paolo Palazzari, ENEA, ICT-HPC division

In memory of Alessandro Marongiu

- He was a reference point in all the workplaces where he worked, both in the public research (ENEA) and in the private (the Ylichron spin-off, PLDA and Accelize).
- He was one of the main architects of the QuickPlay HLS flow.
- He worked for more than 20 years on parallel computing. His main interest has been the automation of the process to translate a high-level description of an algorithm into an equivalent, parallel, lower level description.

Outline of the presentation

- Some preliminary considerations on how to use an HLS flow
- The problem to be solved
- Exploitation of spatial and pipeline parallelism at the different granularities
- Few details on the implementation through the QuickPlay HLS flow
- Performance evaluation
- Conclusions

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float ScalarProduct(float a[N], float b[N]) {
float sum = 0;
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return sum;}
```

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In 5 min (plus ~ 1 hour of compile time) we obtain a working design which computes the scalar product

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- each add is dependent on the result of the previous add;
- we suppose that compiler will be able to overlap the
  - reads from the two memory banks (a[i] and b[i])
  - the a[i-1]*b[i-1] multiply
  - and the sum = sum + result of a[i-2]*b[i-2]

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[illegible] **Latency**$_{Add}$ cycles to be executed

2N-1 operations => ≈ **2/ Latency**$_{Add}$ operations/cycle ≈ 0.5 op/cycle => **100 Mflop/s** (using a typical clock frequency of 200 MHz)

Let’s try to convince them that FPGA can be a good solution once they understand that they must change their mind as they are using a different technology…

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- The Matrix-Vector Multiplication (MVM) is the core of the Wavefront Reconstruction control algorithm.

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PP1

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Diapositiva 20

PP1 Paolo Palazzari; 06/06/2020

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- Computing speed = $\frac{\#\text{Operations}}{\#\text{Cycles to compute MVM}} = \frac{2\text{N}}{\frac{4\text{N}}{\text{BW}}} = \frac{\text{BW}}{2}$

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- It's well known that MVM is limited by the available memory bandwidth; as discussed in the paper, the computational speed in the MVM cannot be larger than **half of the bandwidth** between the FPGA and the external memory;
- Our design is targeting a FPGA board with an Intel ARRIA 10 GX1150 FPGA, with 4 HMC memory banks; the BW toward each bank is 17 GB/s so we know that MVM implementation could not sustain more than **34 Gflop/s**

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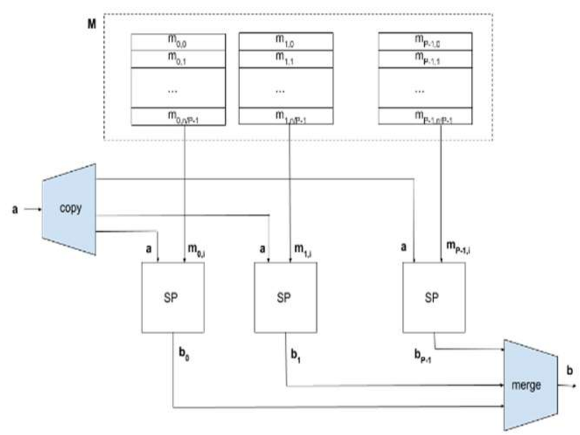
- The sketch of the architecture to be implemented is the following



Pipelined implementation of the scalar product

- The scalar product can be implemented with one pipelined MADD (one multiplier and one adder) which iteratively computes the recurrence

$s_{i+1} = a_i \times b_i + s_i$ $\quad\quad$ $i=0, ..., N-1$ with $s_0=0$, $a_i \in \mathbf{a}$, $b_i \in \mathbf{b}$.

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- As the computation of the next MADD operation is dependent on the completion of the previous operation, a new MADD cannot start until the previous has finished
- Each time we must wait L cycles (the latency of the MADD operator) before starting a new MADD operation

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- The final result is computed summing the L ps_i values. This additional sum requires O(log(L)) cycles and is negligible when N >> L

Fine-grained spatial parallelism

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- To increase the used memory BW we partition each of the L sub-vectors into P smaller sub-vectors $\mathbf{ssa_{ij}}$ and $\mathbf{ssb_{ij}}$

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- The LP partial scalar products are all independent: at each cycle, each scalar product reads P elements from the matrix (and P from the vector which is permanently stored in the local memory)

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- P is the fine-grained spatial parallelism. The value of P is set to saturate the memory BW, i.e.

$4Pf_{ck} = Mem_{BW} \Rightarrow P = \frac{Mem_{BW}}{4f_{ck}}$ (to be rounded at a power of 2)

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  $4Pf_{ck} = Mem_{BW}$ => $P = \frac{Mem_{BW}}{4f_{ck}}$ (to be rounded at a power of 2)

- With Mem_{BW} = 17 GB/s and f_{ck}= 150 MHz we get

  P = 28 => round to **32**

- In each kernel we start, at each clock cycle, 32 MADD operations.

Fine-grained spatial parallelism

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- Once the LP partial scalar products have been computed (in N/P + L – 1 clock cycles), all these values must be summed together
- Using P_A adders having latency L_A, the number of cycles to sum n=LP numbers is given by

$$NCycles_{sum}(P_A) = \sum_{i=1}^{\lceil \log_2(n) \rceil} \left(\left\lceil \frac{n}{2^i} \frac{1}{P_A} \right\rceil + L_A \right) \approx \frac{n}{P_A} + \lceil \log_2(n) \rceil L_A$$

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- From previous expression we get the number of cycle to compute a scalar product

$$\mathrm{NCycles_{SP}} \approx \frac{\mathrm{N}}{\mathrm{P}} + \mathrm{L} + \frac{\mathrm{LP}}{\mathrm{P_A}} + \lceil \log_2(\mathrm{LP}) \rceil \mathrm{L_A}$$

Coarse-grained pipelining

- In the operation **b** = **M** x **a**, the result vector **b** can be computed through

```
for (l=0; l<N; l++){
 load m_l from the external memory
 compute the LP partial scalar products s_ij
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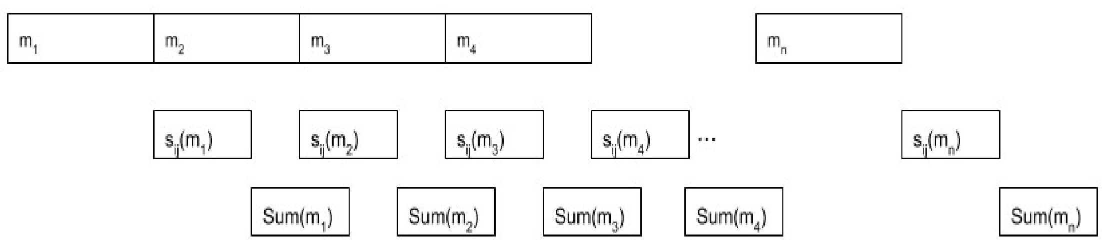
- as the loop iterations are independent, they can be pipelined with the following schedule



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The MADD operator (with fine grained-spatial parallelism)

```
/*#qp pipeline */
Void MADD(float a1,…a32, float b1,…b32,float &c1,… &c32)
{
 c1 += a1*b1;
 …
 c32 += a32*b32;
}
```

The scalar product (fine-grained pipelined and spatial parallelism)

```
count=0;…,count31=31; //init the 32 count vars
/*#qp unroll 32*/
for (i=0; i<(N)/(L*P); i++){
 // 1st value
 a1 = a[count];   …   a32 = a[count31];
 b1 = b[count];   …   b32 = b[count31];

 MADD(a1, …,a32,b1,…,b32,s0_0,…,s0_31);

 Inc(count,…,count31);
 …

 // Lth value
 a1 = a[count];   …   a32 = a[count31];
 b1 = b[count];   …   b32 = b[count31];

 MADD(a1,…,a32,b1,…,b32,s7_0,…,s7_31);
 Inc(count,…,count31);
}
```

The sum function

```
float Sum(float s0_0,..., float s7_31)
{
	float result;
	result =s0_0+s0_1+...+s0_31+s1_0+...+s7_31; //256 operands
	return result;
}
```

MVM with corse-grained pipelining

The preamble

```
qpReadStream(d_in_0,a1,NbElem*sizeof(float));//read vect a

ReadVector(b1, Matrix,row);    row++; // read a row of M
ComputePartialScalarProducts(a1, b1, cr0_0,..., cr0_31);
sum1 = Sum(cr0_0,..., cr0_31);
ReadVector(b2, Matrix, row);   row++;
ComputePartialScalarProducts(a1, b2, cr0_0,..., cr0_31);
ReadVector(b3, Matrix, row);  row++;
```

MVM with corse-grained pipelining

The main body

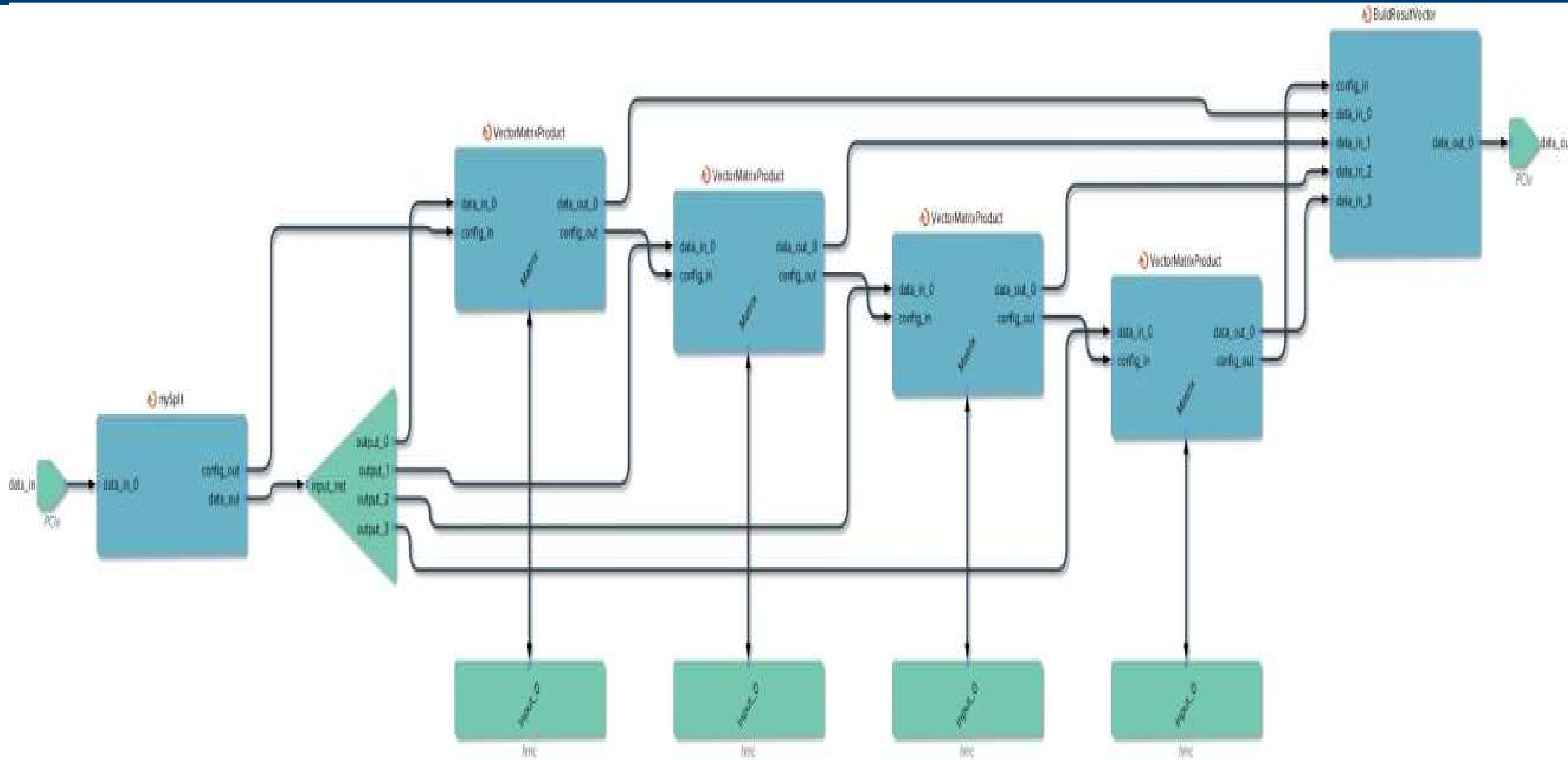
```
for (i=0; i<myNbProducts-6; i+=3)    {
        Write(dout,sum1,false); //send an element of the result vector
        sum2 = Sum(cr0_0,..., cr0_31);
        Write(dout,sum2,false);
        ComputePartialScalarProducts(a1, b3, cr0_0,..., cr0_31);
        sum3 = Sum(cr0_0,..., cr0_31);
        Write(dout,sum3,false);
        ReadVector(b1, Matrix, row);  row++;
        ComputePartialScalarProducts(a1, b1, cr0_0,..., cr0_31);
        sum1 = Sum(cr0_0,..., cr0_31);
        ReadVector(b2, Matrix, row);   row++;
        ComputePartialScalarProducts(a1, b2, cr0_0,..., cr0_31);
        ReadVector(b3, Matrix, row);  row++;}
```

MVM with corse-grained pipelining

The postamble

```
Write(dout,sum1,false);
i++;  // i is the number of written values
sum2 = Sum(cr0_0,..., cr0_31);
Write(dout,sum2,false);
i++;  // i is the number of written values
ComputePartialScalarProducts(a1, b3, cr0_0,..., cr0_31);
sum3 = Sum(cr0_0,..., cr0_31);
Write(dout,sum3,i==NbProducts-1);
```

The whole design



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Performance

	1 Kernel	2 Kernels	3 Kernels	4 Kernels
Speed [GFlop/s]	5.3	10.6	15.9	21.0
ALM	88547	190648	264600	282473
M20K	500	959	1378	2045

Performance

- The 21 Gflop/s is below the expected limit, fixed by the available memory BW (34 Gflop/s)
- Going more in depth, we see that the number of cycles needed to transfer data from the external memory to the FPGA internal memory is given by

$$N_{mem} = \frac{N}{P} + L_m$$

where L_m= 200 cycles. As N/P in our case is 256, the latency is comparable with the transfer time.

Therefore we see a memory BW = $f_{ck} \frac{4N}{\frac{N}{P}+L_m} \approx 11 \frac{GB}{s}$ which corresponds to the computing speed of 5.5 Gflop/s, in good agreement with the achieved performance (5.3 Gflop/s with one kernel).

Performance

- In order to achieve the expected performance (8.5 Gflop/s for each kernel), we should be able to overlap the latency of the memory read for the transfer of one line of the matrix with the actual transfer of the previous line.

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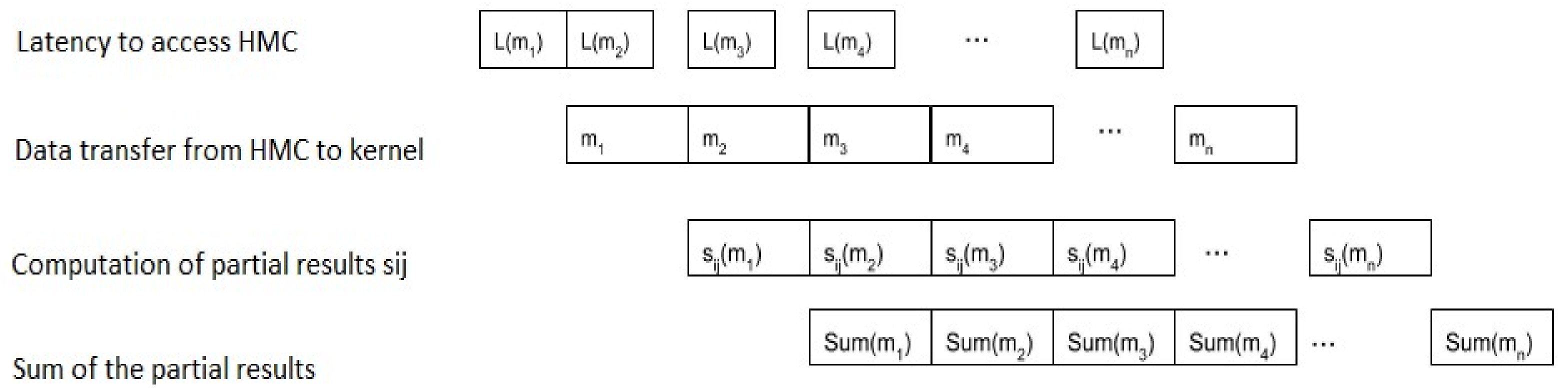

Outline of the presentation

- Some preliminary considerations on how to use an HLS flow
- The problem to be solved
- Exploitation of spatial and pipeline parallelism at the different granularities
- Few details on the implementation through the QuickPlay HLS flow
- Performance evaluation
- Conclusions

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Conclusions

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- We showed the necessity to be aware of the different kind of parallelism in order to efficiently exploit them
- In this case, we used both pipeline and spatial parallelism at the fine-grain and at the coarse grain
- We exposed our idea that HLS should not abstract us too much from the actual architecture, as we should be able to foresee which should be the performance achievable and the performance of the actual HLS implementation of a given algorithm should be evaluated against this theoretical prediction
- We discourage as much as possible performance evaluation through comparison with other implementations

- Thank you for your attention

- For any information, feel free to contact me at

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